REMARKS/ARGUMENTS

In the Office Action dated September 9, 2005, Examiner rejected claims 1-4, 6, 7, 8, 10-12, 15 and 17 under 35 U.S.C.§ 102(e) as anticipated by Nauget (USPN 6,377,644), and claim 14 is rejected under 35 U.S.C. §103(a) as unpatentable over Nauget.

Applicant appreciates that the examiner found claims 5, 9, 13 and 16 to be allowable if rewritten, however, respectfully traverse the rejection of the base claims at least for the following reason.

Despite the apparent similarity between the present invention and the technique described in US Patent 6 377 644 (Naudet) Applicant submits that there are crucial and fundamental differences which render the substitution of the present invention into a system using the technique described in Naudet impractical.

One key difference is that the present invention is preferably implemented as part of a Field Programmable Gate Array (FPGA) device. Accordingly, there is a finite limit to the upper operating frequency of such a device. As a result of this the inventor arrived at the invention in order to achieve the measurement of phase jitter without a high frequency sampling rate using a lower frequency with a known frequency offset. Such an implementation could not be achieved using the principles described and claimed by Naudet. The obviousness objection is therefore strongly refuted.

Reasons why the present invention is both novel and inventive over Naudet are further set out below.

An object of the present invention is to measure the amount of phase jitter. This is important for network service managers and content providers, as there are standards and recommendations specified for the allowable amount of jitter. Excess jitter has a detrimental effect on performance and operators can be penalised under service contracts.

Superficially, the description in Naudet of a frequency offset appears to be similar to the method of the present invention. However, upon closer scrutiny, the implementation of clock signals by Naudet and the way in which the invention works are completely different.

The method described by Naudet requires the clock signals to be fed, via a delay line, so that multiple clocking signals are produced, each with a fixed phase offset from the previous. These clocks are then used to produce multiple 'offset' samples which can be processed just as if all of these samples were taken using a single clock running at a higher speed. A Reverse Fourier Transform is then performed by Naudet, this is a form of Digital Signal Processing (DSP), which requires a complex processing unit.

In contrast, the method of the present invention employs **a single-phase clock** and does not use any phase shifted clocks. Instead, the present invention uses counters that operate in real time. Therefore, the expense of Reverse Fourier Transforms and Digital Signal Processing are avoided and no calculations need to be performed, thus avoiding further expense of complex processing software.

The present technique employs a reference clock signal, whose frequency is chosen so that it has an offset from the input signal clock (**n:m**). The reason for this is that the clock and the input signals therefore only have the same phase relationship once ever **n** cycles of a reference clock (which equals **m** cycles of the input signal clock) because the ratio of the reference clock to the input signal is **n:m**, where m and n are integers. If there is jitter present on the input signal then the number of cycles that the 'same-phase relationship' occurs will be different from the ideal number (**n**). The value in the counter indicates this position and no processing or Reverse Fourier Transforms are necessary.

The present invention further employs an edge detector to synchronise an initial phase relationship between the clock signal and the input signal by disabling the circuit until this phase relationship occurs. Once synchronised, the counter is enabled and, when the two signals are again 'in sync' one with another, the counter value is stored. The counter wraps and counting is repeated continuously. At the end of each period the value in the counter is compared with the max/min registers, and, if these are exceeded, they are updated and therefore the peaks of the jitter are retained. At the end of a measurement period a precise measurement of the peak-to-peak phase jitter is obtained by simply reading the max and min registers. This is achieved for example by counters arranged to detect a fixed (predetermined) phase relationship (first occurrence) and then continuously counting the number of reference clock cycles until this phase relationship recurs (subsequent occurrence), as described in a preferred embodiment. The count is compared with the previous counts, and the maximum/minimum values present the amount of jitter. Thus, no calculations need to be performed in the present method for measurement of jitter.

The advantage of the present invention therefore is that the present apparatus and method do not require a frequency higher than the input signal, and/or any expensive multiphase clocks. Thus, the phase jitter measurement may be achieved by using less expensive devices.

Furthermore, because there is no sampling, digital signal processing (DSP) techniques are not required or used in the present method of measurement.

Based on the above explanation, Applicant respectfully submits that claims 1-17 pending in the present application as originally filed are allowable over the prior art and the application is in condition for allowance.

Favorable reconsideration of the rejection of the claims pending in this application is respectfully solicited.

A certified copy of the priority application GB 0026556.1 is submitted concurrently herewith.

The Commissioner is hereby authorized to charge any additional fees which may be required in this application under 37 C.F.R. §§1.16-1.17 during its entire pendency, or credit any overpayment, to Deposit Account No. 06-1135. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, other-wise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1135.

Respectfully submitted,

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